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-- REMARKS --

In the Final Office Action, Examiner Shapiro rejected pending claims 9-12 under 35 U.S.C. §112, ¶1 as containing subject matter which was not described in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the enablement of claims 9-12 as related to "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein each individual signal processing circuit associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on said substrate" as recited in independent claim 9. The Applicant respectfully traverses this 35 U.S.C. § 112, ¶1 rejection of claims 9-12, because the description of FIGS. 1, 2, 4 and 5 reasonably conveys to one skilled in the relevant art that the inventor Mr. Edwards, at the time the application was filed on July 11, 2000, had possession of the invention as claimed in independent claim 9.

The first limitation of claim 9 is a substrate, which is enabled by the description of substrate 25 illustrated in FIGS. 1 and 4.

The second limitation of claim 9 is an array of individually addressable matrix elements carried on the substrate, which is enabled by the description of an array of addressable matrix elements 18 as illustrated in FIG. 1.

The third limitation of claim 9 is a set of address conductors connected to the array of matrix elements and carried on the substrate, which is enabled by the description of a set of address conductors 16 as illustrated in FIGS. 1, 2, 4 and 5.

The fourth limitation of claim 9 is the set of address conductors being arranged in a series of groups with each group including successive address conductors, which is enabled by the description of a group G1 having successive address conductors C1-C9 and a group G2 having successive address conductors C10-C18 as illustrated in FIG. 2.

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The fifth and sixth limitations of claim 9 are a multiplexing circuit integrated on the substrate and connected to the set of address conductors and a plurality of signal bus lines, which are enabled by the description of control circuit 37, switches 32, and video bus lines V1-V9 as illustrated in FIG. 9.

The seventh limitation of claim 9 is the multiplexing circuit being arranged to couple sequentially each group of the set of address conductors to the plurality of signal bus lines with each address conductor in a group being coupled to a respective one of the signal bus lines. This limitation is enabled by the description of group G1 of successive address conductors C1-C9 being coupled to respective video bus lines V1-V9 via switches 32 as illustrated in FIG. 2 and of group G2 of successive address conductors C10-C18 being coupled to respective video bus lines V1-V9 via switches 32 as illustrated in FIG. 2.

The eighth and ninth limitations of claim 9 are a plurality of signal processing circuits integrated on the substrate and each signal processing circuit being connected to a respective bus line. These limitations are enabled by the signal processing circuits 42(1)-42(9) integrated on substrate 25 and being connected to respective bus lines V1-V9 as illustrated in FIGS. 4 and 5.

The tenth and final limitation of claim 9 is each individual signal processing circuit being associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on the substrate. This limitation, as illustrated in FIGS. 2, 4 and 5, is enabled by the description of (1) signal processing circuit 42(1) being associated with the first address conductor C10 of group G2 due to the coupling of bus line V1 to address conductor C10, (2) signal processing circuit 42(9) being associated with the last address conductor C9 of group G1 due to the coupling of bus line V9 to address conductor C9, and (3) signal processing circuits 42(1) and 42(9) being adjacent on substrate 25. The Applicant has amended claim 9 herein to recite "wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" to point out that the groups are related to the address conductors and not the signal processing circuits.

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Withdrawal of the rejection of claims 9-12 under 35 U.S.C. §112, ¶1 as containing subject matter which was not described in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention is therefore respectfully requested.

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SUMMARY

Examiner Shapiro's 35 U.S.C. §112, ¶1 of claims 9-12 has been obviated by the remarks supporting the enablement of claims 9-12. The Applicant respectfully submits that claims 9-12 as amended herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, Examiner Shapiro is respectfully requested to contact the undersigned at the telephone number listed below.

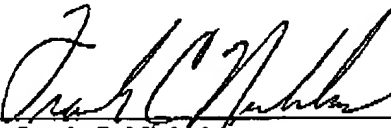
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